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Title

METHOD AND SISTEM FOR ATTENUATING THE FAULTS THAT APPEAR IN DATA PROCESSING UNITS IMPLEMENTED USING DIGITAL CIRCUITS

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Short presentation

The patent refers to a method and system for mitigating probabilistic errors that occur in digital circuit implementations where the data processing is based on addition, multiplication, and accumulation operations or can be decomposed into such operations. The system consists of two instances of the data processor connected in parallel, each consisting of the one hand of the block that implements the procedure, usually a mathematical rule, and on the other hand of the block for calculating the correction input, each having access and using the results produced by the other circuit. The method, according to the invention, involves the creation of a dynamic model that describes the current state of the circuit and the calculation of correction factors based on this model.

Applicability

The method can be used to mitigate probabilistic errors that occur in implementations of digital integrated circuits in computing systems on data paths that use add, multiply, and accumulate operations. It can also be used only for the purpose of detecting defects, without mitigating them.

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